specification, Applicant's construction permits bonding both the bonding pad of the lower chip and the wiring pattern on the wiring sheet to the bonding pad of the package substrate in a single wire bonding step. Yet another advantage, as discussed in the first full paragraph of page 6 in the original specification, is that this also permits size reduction both in terms of package thickness and in the horizontal direction. Accordingly, it is submitted that none of the art alone or in combination reasonably could be said to anticipate or render obvious the claimed invention.

Pursuant to 37 CFR 1.121, marked copies of the specification paragraph and amended claims showing changes made therein accompany this amendment. No new matter has been entered.

In the event there are any fee deficiencies or additional fees payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

In the event the Examiner desires personal contact for further disposition of this case, the Examiner is invited to contact the undersigned attorney at (520) 882-7623.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on August 2, 2002 at Tucson, Arizona.

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MARKED COPY OF SPECIFICATION PARAGRAPH

SERIAL NO. 09/593,891

DOCKET: NEC DP-624

MARKED SPECIFICATION PARAGRAPH SHOWING CHANGES MADE

Paragraph beginning at page 5, line 17:

Next, there will be described the second embodiment of the present invention. In the above-described first embodiment, the construction places the rear surface of the upper chip 3 on the surface of the wiring sheet 9. However, in the present embodiment, the upper chip 3 is placed on the wiring sheet 9 in such a way that chip surface is directed to the lower direction while causing inside and outside to be reversed, i.e., upside-down, before placing on the wiring sheet 9. Further, one end of the wiring pattern 14 of the wiring sheet 9 is connected directly to the bonding pad 4 of the upper chip 3, while the other end of the wiring pattern 14 is connected to the bonding pad 7 of the lower chip 2.

MARKED COPY OF AMENDED CLAIM

SERIAL NO. 09/593,891

DOCKET: NEC DP-624

MARKED CLAIMS SHOWING CHANGES MADE

1. (Thrice Amended) A stacked semiconductor storage device comprising, in combination, a lower chip and an upper chip superimposed on a substrate, said semiconductor storage device further comprising:

a wiring substrate having wiring patterns thereon, interposed between said lower chip and said upper chip, for relaying electric connection between bonding pads on said upper chip and bonding pads on said substrate, wherein the bonding pads on said upper chip are arranged in a line running perpendicular to a line of bonding pads on the substrate[.];

wherein said upper chip has an upper and a lower surface, said lower surface facing said substrate; and

wherein the bonding pads on said upper chip that connect to the bonding pads of said substrate are disposed on the lower surface of said upper chip.